AMENDMENTS TO THE CLAIMS:

1. (Previously Presented) An M-bit adder capable of receiving a first M-bit argument, a second M-bit argument, and a carry-in (CI) bit comprising:

M adder cells arranged in R rows, wherein a least significant adder cell in a first one of said rows of adder cells is operable to:

receive a first data bit, A_X, from said first M-bit argument and a first data bit, B_X, from said second M-bit argument,

generate both a first conditional carry-out bit, $C_X(1)$, and a second conditional carry-out bit, $C_X(0)$,

provide the first and second conditional carry-out bits $C_X(1)$ and $C_X(0)$ to a second one of said adder cells, and

wherein said $C_X(1)$ bit is calculated assuming a row carry-out bit from a second row of adder cells preceding said first row is a 1 and said $C_X(0)$ bit is calculated assuming said row carry-out bit from said second row is a 0; and

wherein said second one of said adder cells in said first one of said rows is operable to:

receive a first data bit, A_{X+1}, from said first M-bit argument and a first data bit, B_{X+1}, from said second M-bit argument,

receive both said first conditional carry-out bit, $C_X(1)$ and said second conditional carry-out bit, $C_X(0)$;

generate both a first conditional carry-out bit, $C_{X+1}(1)$, and a second conditional carry-out bit, $C_{X+1}(0)$ by propagating said first conditional carry-out bit, $C_X(1)$ and said second conditional carry-out bit, $C_X(0)$ through a first pass gate and a second pass gate, respectively, when said first data bit A_{X+1} and said second data bit B_{X+1} are not equal, and

output said first and second conditional carry-out bits $C_{X+1}(1)$ and $C_{X+1}(0)$ to other circuitry.

2. (Original) The M-bit adder as set forth in Claim 1 wherein said least significant adder cell generates a first conditional sum bit, $S_X(1)$, and a second conditional sum bit, $S_X(0)$.

3. (Original) The M-bit adder as set forth in Claim 2 wherein said $S_X(1)$ bit is calculated assuming said row carry-out bit from said second row is a 1 and said $S_X(0)$ bit is calculated assuming said row carry-out bit from said second row is a 0.

4. (Original) The M-bit adder as set forth in Claim 3 wherein said row carry-out bit selects one of said $S_X(1)$ bit and said $S_X(0)$ bit to be output by said least significant adder cell.

5. (Previously Presented) The M-bit adder as set forth in Claim 4 wherein said other circuitry comprises:

a third adder cell in said first one of said rows of adder cells, and wherein said third adder cell receives a third data bit, A_{X+2}, from said first M-bit argument and a third data bit, B_{X+2}, from said second M-bit argument, and receives from said second adder cell said $C_{X+1}(1)$ bit and said $C_{X+1}(0)$ bit.

6. - 7. (Canceled).

8. (Previously Presented) The M-bit adder as set forth in Claim 4 wherein said second adder cell generates a first conditional sum bit, $S_{X+1}(1)$, wherein said $S_{X+1}(1)$ bit is generated from said A_{X+1} data bit, said B_{X+1} data bit, and said $C_X(1)$ bit from said least significant adder cell.

9. (Original) The M-bit adder as set forth in Claim 8 wherein said second adder cell generates a second conditional sum bit, $S_{X+1}(0)$, wherein said $S_{X+1}(0)$ bit is generated from said A_{X+1} data bit, said B_{X+1} data bit, and said $C_X(0)$ bit from said least significant adder cell.

10. (Original) The M-bit adder as set forth in Claim 9 wherein said row carry-out bit selects one of said $S_{X+1}(1)$ bit and said $S_{X+1}(0)$ bit to be output by said second adder cell.

11. (Original) The M-bit adder as set forth in Claim 1 wherein said first row of adder cells contains N adder cells and said second row of adder cells preceding said first row contains less than N adder cells.

12. (Previously Presented) A data processor comprising:

an instruction execution pipeline comprising N processing stages, each of said N processing stages capable of performing one of a plurality of execution steps associated with a pending instruction being executed by said instruction execution pipeline, wherein at least one of said N processing stages comprises an M-bit adder capable of receiving a first M-bit argument, a second M-bit argument, and a carry-in (CI) bit, said M-bit adder comprising:

M adder cells arranged in R rows, wherein a least significant adder cell in a first one of said rows of adder cells is operable to:

receive a first data bit, A_X, from said first M-bit argument and a first data bit, B_X, from said second M-bit argument,

generate both a first conditional carry-out bit, $C_X(1)$, and a second conditional carry-out bit, $C_X(0)$,

provide the first and second conditional carry-out bits $C_X(1)$ and $C_X(0)$ to a second one of said adder cells, and

wherein said $C_X(1)$ bit is calculated assuming a row carry-out bit from a second row of adder cells preceding said first row is a 1 and said $C_X(0)$ bit is calculated assuming said row carry-out bit from said second row is a 0; and

wherein said second one of said adder cells in said first one of said rows is operable to:

receive a first data bit, A_{X+1}, from said first M-bit argument and a first data bit, B_{X+1}, from said second M-bit argument,

receive both said first conditional carry-out bit, $C_X(1)$ and said second conditional carry-out bit, $C_X(0)$;

generate both a first conditional carry-out bit, $C_{X+1}(1)$, and a second conditional carry-out bit, $C_{X+1}(0)$ by propagating said first conditional carry-out bit, $C_X(1)$ and said second conditional carry-out bit, $C_X(0)$ through a first pass gate and a second pass gate, respectively, when said first data bit A_{X+1} and said second data bit B_{X+1} are not equal, and

output said first and second conditional carry-out bits $C_{X+1}(1)$ and $C_{X+1}(0)$..

13. (Original) The data processor as set forth in Claim 12 wherein said least significant adder cell generates a first conditional sum bit, $S_X(1)$, and a second conditional sum bit, $S_X(0)$.

14. (Original) The data processor as set forth in Claim 13 wherein said $S_X(1)$ bit is calculated assuming said row carry-out bit from said second row is a 1 and said $S_X(0)$ bit is calculated assuming said row carry-out bit from said second row is a 0.

15. (Original) The data processor as set forth in Claim 14 wherein said row carry-out bit selects one of said $S_X(1)$ bit and said $S_X(0)$ bit to be output by said least significant adder cell.

16. (Previously Presented) The data processor as set forth in Claim 15 wherein said other circuitry comprises:

a third adder cell in said first one of said rows of adder cells, and wherein said third adder cell receives a third data bit, A_{X+2}, from said first M-bit argument and a third data bit, B_{X+2}, from said second M-bit argument, and receives from said second adder cell said $C_{X+1}(1)$ bit and said $C_{X+1}(0)$ bit.

17. - 18. (Canceled).

19. (Previously Presented) The data processor as set forth in Claim 15 wherein said second adder cell generates a first conditional sum bit, $S_{X+1}(1)$, wherein said $S_{X+1}(1)$ bit is generated from said A_{X+1} data bit, said B_{X+1} data bit, and said $C_X(1)$ bit from said least significant adder cell.

20. (Original) The data processor as set forth in Claim 19 wherein said second adder cell generates a second conditional sum bit, $S_{X+1}(0)$, wherein said $S_{X+1}(0)$ bit is generated from said A_{X+1} data bit, said B_{X+1} data bit, and said $C_X(0)$ bit from said least significant adder cell.

21. (Original) The data processor as set forth in Claim 20 wherein said row carry-out bit selects one of said $S_{X+1}(1)$ bit and said $S_{X+1}(0)$ bit to be output by said second adder cell.

22. (Original) The data processor as set forth in Claim 12 wherein said first row of adder cells contains N adder cells and said second row of adder cells preceding said first row contains less than N adder cells.

23. (Previously Presented) A method of adding a first M-bit argument and a second M-bit argument in an M-bit adder, the M-bit adder comprising M adder cells arranged in R rows, the method comprising the steps of:

receiving a first data bit, A_X, from the first M-bit argument and a first data bit, B_X, from the second M-bit argument in a least significant adder cell in a first one of the rows of adder cells;

calculating in the least significant adder cell a first conditional carry-out bit, $C_X(1)$, assuming a row carry-out bit from a second row of adder cells preceding the first row is a 1;

calculating in the least significant adder cell a second conditional carry-out bit, $C_X(0)$, assuming the row carry-out bit from the second row is a 0;

calculating in the least significant adder cell a first conditional sum bit, $S_X(1)$, assuming the row carry-out bit from the second row is a 1;

calculating in the least significant adder cell a second conditional sum bit, $S_X(0)$, assuming the row carry-out bit from the second row is a 0;

propagating the $C_X(1)$ bit and the $C_X(0)$ bit to a second adder cell in the first row of adder cells;

selecting one of the $S_X(1)$ bit and the $S_X(0)$ bit to be output from the least significant adder cell according to a value of the row carry-out bit from the second row; and.

receiving a first data bit, A_{X+1}, from the first M-bit argument and a first data bit, B_{X+1}, from the second M-bit argument in the second adder cell in said first one of said rows of adder cells;

generating in said second adder cell both a first conditional carry-out bit, $C_{X+1}(1)$, and a second conditional carry-out bit, $C_{X+1}(0)$ by propagating said first conditional carry-out bit $C_X(1)$ and said second conditional carry-out bit $C_X(0)$ through a first pass gate and a second pass gate, respectively, when said first data bit A_{X+1} and said second data bit B_{X+1} are not equal, and

outputting said first and second conditional carry-out bits $C_{X+1}(1)$ and $C_{X+1}(0)$ to other circuitry.

24. (Previously Presented) The M-bit adder as set forth in Claim 1 wherein said second adder cell further comprises:

a first inverter operable for inverting said first conditional carry-out bit $C_X(1)$ transmitted through said first pass gate prior to outputting said first conditional carry-out bit $C_X(1)$; and

a second inverter operable for inverting said second conditional carry-out bit $C_X(0)$ transmitted through said second pass gate prior to outputting said second conditional carry-out bit $C_X(0)$.

25. (Previously Presented) The M-bit adder as set forth in Claim 1 wherein said second adder cell further comprises:

a first inverter operable for inverting said received conditional carry-out bit $C_X(1)$ prior to transmission through said first pass gate; and

a second inverter operable for inverting said received second conditional carry-out bit $C_X(0)$ prior to transmission through said second pass gate.

26. (Previously Presented) The M-bit adder as set forth in Claim 1 wherein said other circuitry comprises:

a row multiplexer, wherein said row carry-out bit from said second row of adder cells preceding said first row selects one of said $C_{X+1}(1)$ bit and said $C_{X+1}(0)$ bit to be output by said row multiplexer.

27. (Previously Presented) The M-bit adder as set forth in Claim 9 wherein said first adder cell comprises:

a first multiplexer operable for receiving said first conditional sum bit, $S_X(1)$ and said second conditional sum bit $S_X(0)$, wherein said row carry-out bit selects one of said $S_X(1)$ bit and said $S_X(0)$ bit to be output by said first adder cell; and

said second adder cell comprises:

a second multiplexer operable for receiving said second conditional sum bit $S_{X+1}(1)$ and said second conditional sum bit $S_{X+1}(0)$, wherein said row carry-out bit selects one of said $S_{X+1}(1)$ bit and said $S_{X+1}(0)$ bit to be output by said second adder cell.

28. (Previously Presented) The data processor as set forth in Claim 12 wherein said second adder cell further comprises:

a first inverter operable for inverting said first conditional carry-out bit $C_X(1)$ transmitted through said first pass gate prior to outputting said first conditional carry-out bit $C_X(1)$; and

a second inverter operable for inverting said second conditional carry-out bit $C_X(0)$ transmitted through said second pass gate prior to outputting said second conditional carry-out bit $C_X(0)$.

29. (Previously Presented) The data processor as set forth in Claim 12 wherein said second adder cell further comprises:

a first inverter operable for inverting said received conditional carry-out bit $C_X(1)$ prior to transmission through said first pass gate; and

a second inverter operable for inverting said received second conditional carry-out bit $C_X(0)$ prior to transmission through said second pass gate.

30. (Previously Presented) The data processor as set forth in Claim 12 wherein said other circuitry comprises:

a row multiplexer, wherein said row carry-out bit from said second row of adder cells preceding said first row selects one of said $C_{X+1}(1)$ bit and said $C_{X+1}(0)$ bit to be output by said row multiplexer.

31. (Previously Presented) The data processor as set forth in Claim 20 wherein said first adder cell comprises:

a first multiplexer operable for receiving said first conditional sum bit, $S_X(1)$ and said second conditional sum bit $S_X(0)$, wherein said row carry-out bit selects one of said $S_X(1)$ bit and said $S_X(0)$ bit to be output by said first adder cell; and

said second adder cell comprises:

a second multiplexer operable for receiving said second conditional sum bit $S_{X+1}(1)$ and said second conditional sum bit $S_{X+1}(0)$, wherein said row carry-out bit selects one of said $S_{X+1}(1)$ bit and said $S_{X+1}(0)$ bit to be output by said second adder cell.